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What's Inside

Haptic Rendering of Cultural Heritage Objects

Sreeni K.G. (Research Scholar), Praseedha Krishnan, Priyadarshini Kumari (both pursuing M. Tech) From Vision and Image Processing Lab under the guidance of Prof. Subhasis Chaudhuri

"*People without the knowledge of their past history, origin and culture is like a tree without roots.*" These words of the famous journalist and entrepreneur Marcus Garvey reflect the significance of culture in human lives. However, armed conflicts and war, earthquakes and other natural disasters, pollution, uncontrolled urbanization and unchecked tourist development pose major threats to world heritage sites. Therefore, as UNESCO remarks in its Draft Medium Term Plan 1990-1995, the preservation and the presentation of the cultural heritage should be the corner-stone of any cultural policy. In the recent years, digital technology is paving a way into safeguarding cultural heritages, and it also offers a great promise for enhancing access to them. A user's experience of accessing such cultural objects can be made more realistic and immersive by incorporating the recently evolving haptic technologies.

Haptics is a term that was derived from the Greek verb haptesthai meaning relating to the sense of touch. In the early nineties, virtualized haptics or "computer haptics" became possible with the emergence of new technologies. Just as computer graphics is concerned with synthesizing and rendering visual images, computer haptics is the science of developing software algorithms that synthesize computer generated forces to be fed back to the user for manipulation of virtual objects through touch. This process of computing and generating forces in response to user interactions with virtual objects is termed as 'haptic rendering'.

We, at Vision and Image Processing lab, are part of a "Cutural Heritage Project" launched by the Government of India. Our main focus is to provide access of artistic objects of any physical scale to the differently abled people. This technique can also provide a better immersive experience even to people with proper eye sight. Different IITs are contributing to this project. A team from IIT Delhi has been constructing the 3D model of various cultural heritage objects like the pillars in Hampi, Taj Mahal, etc. We, at IIT Bombay, have developed techniques to touch these virtual 3D models at various zoom / scale levels so that the user can experience the object at various levels of detail. The easy availability of very high resolution images as in Digital Michelangelo Project archive enabled us to experiment with various point cloud data, often leading to a more accurate haptic force rendering.

The 3D model taken here is a set of well arranged points representing the surface of the object. The implemented algorithm checks if there is a collision between the user's exploration point (called as proxy. It is similar to a cursor on a screen in 2D) and the 3D object. If a collision is detected, the depth of penetration into the object is calculated. A force is fed back to the user through a haptic device. This force is proportional to the penetration depth and is also dependent on the material properties of the object. ■

3D Data Courtesy: www.archibaseplanet.com.

Figures above show parts of a 3D model being selected at various levels of detail. With a haptic device, the model can actually be touched and felt!

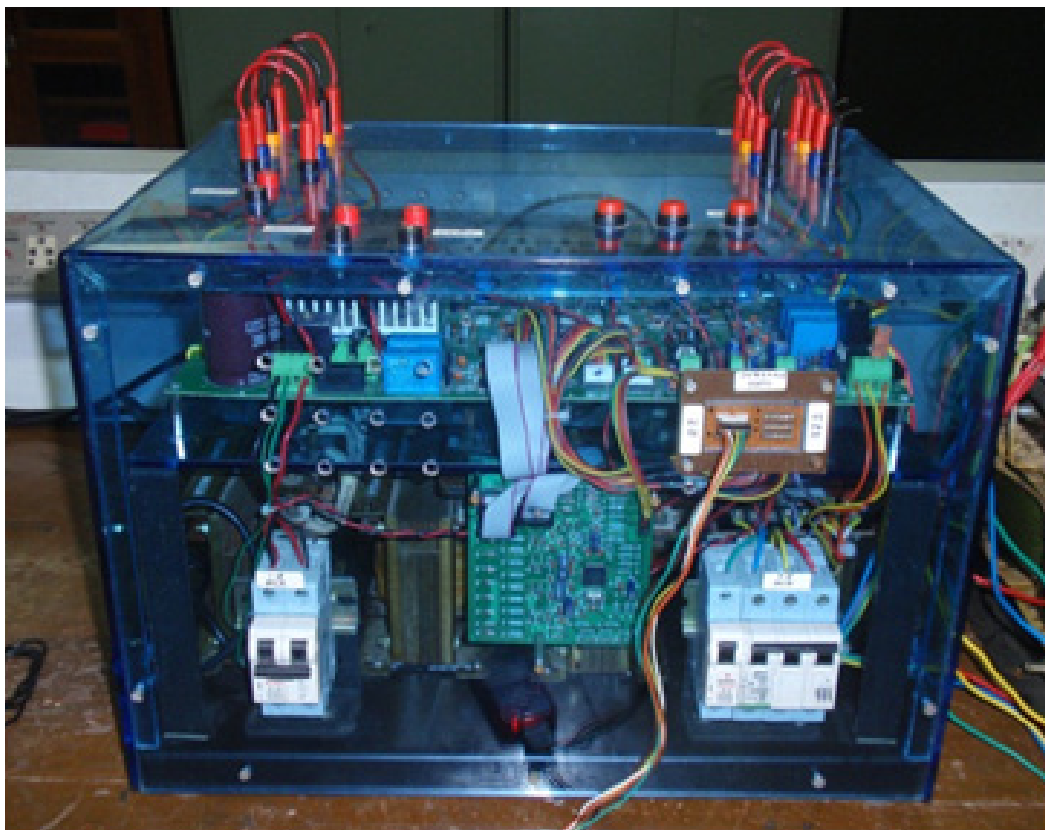
Power Electronics and Drives Experiment Bench (PEDEB)

Rajesh S. Farswan, Sandeep Anand (Research Scholars in Power Electronics1 Lab under Prof. B.G. Fernandes)

The power electronics and drives equipment which is being used in educational and research laboratories has limited flexibility. Only a few experiments can be performed with these benches. Therefore, a large variety of equipment is required for a laboratory course on Power Electronics and Electric Drives which demands high investment. Therefore, a low cost and versatile test bench is the need of the hour.

In order to address this need, a low cost Power Electronics and Drives Experiment Bench (PEDEB) is developed, and is shown in fig.1. Around 30 experiments on power electronics and induction motor drive can be performed utilising 11 circuit topologies available in one bench.

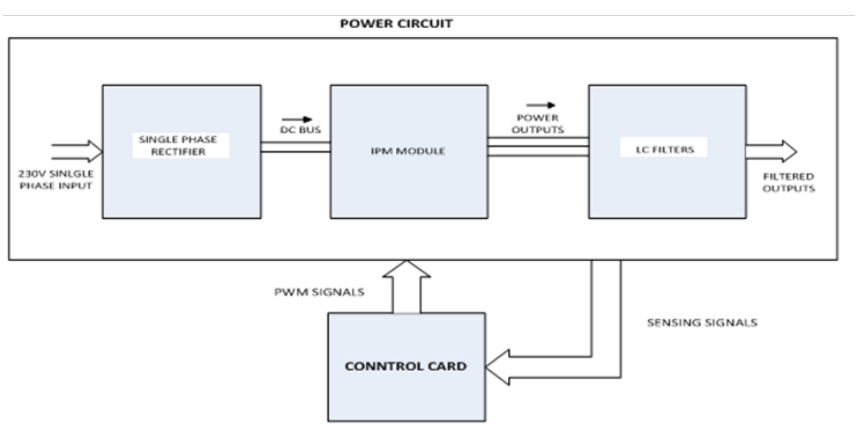
The power circuit consists of a single phase ac-dc converter stage which generates dc link voltage for Integrated Power Circuit Module (IPM). This module has three single -phase half-bridge legs of Insulated Gate Bipolar Transistor (IGBT). Depending upon the requirement, the output of IPM can be configured externally. The pulse width modulated output of the IPM can be filtered using LC filter. The Basic block diagram of PEDEB is shown in fig. 2.

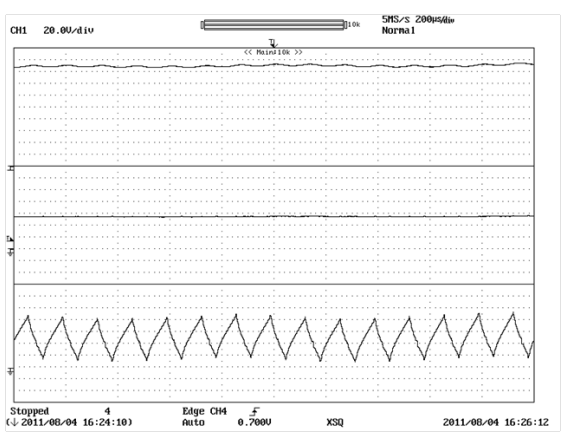


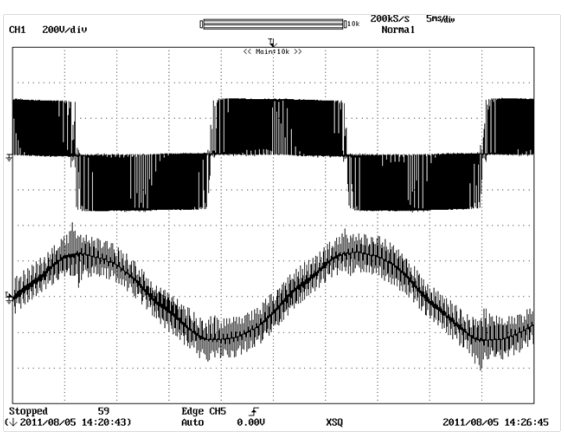
All the control signals and the secondary protection are implemented on a microcontroller based control card. The control parameters can be changed or adjusted on-line using software to emulate the various practical conditions. The control signals generated by the microcontroller and various voltage and current waveforms are available on the module. An ordinary storage oscilloscope can be used to view these waveforms. The primary protection for the IPM against any faults is implemented on hardware.

As an example, the IPM is configured as a buck dc-dc converter and the waveforms of output voltage, output current and inductor current are shown in fig.3. Fig.4 shows the induction motor phase voltage and current waveforms when it is driven by this test bench. Sinusoidal PWM technique is used to vary the voltage applied to the motor so that V/F is held constant.

In addition, experiment showing feeding power either from wind or solar to the grid can also be demonstrated using this bench. Thus PEDEB can be used to set up a full semester laboratory course on power electronics and drives. It can be also used by the research scholars for fast proof of concept. ■







A Tour of the VLSI Lab (Part I)!

Prof. M. Shojaei Baghini, Marshnil Dave, Neha Karanjkar

This article is an attempt to familiarize the readers with the current research activities at VLSI Lab in our department. VLSI Lab has maintained high standards in its research work and related academic curricula. This may be evident from the many accolades won by students in various global design competitions in recent years. The lab maintains diversity in the research work right from system level to the circuit level. Here, we have tried to present a few projects presently being undertaken at the lab.
The following faculty members, listed in alphabetical order, contribute to the research activities and administration of VLSI lab.

Professors A. N. Chandorkar, M. P. Desai, Shalabh Gupta, J. Mukherjee, H. Narayanan, S. Patkar, , D. K. Sharma and M. Shojaei Baghini

It's worth to mention that VLSI lab RAs take care of installation and administration of EDA tools, user accounts, hardware, servers and networking of the lab. Moreover research activities of VLSI lab are results of projects being achieved by many interested and encaustic Ph.D, M.Tech., Dual Degree and B. Tech. students.

The remaining part of this article provides a glimpse of research activities in VLSI lab. Projects are listed as per alphabetical order of their title.

High-Level Synthesis

Faculty Involved: Prof. M. P. Desai

Current digital VLSI circuits can contain billions of transistors and this number is likely to grow. The rising complexity achievable in ASICs presents challenges in design and verification. High level synthesis is one way to handle this complexity. High level synthesis is the process of generating hardware from high level programs. For example, given the functionality of a system described as an executable C program, a high level synthesis flow generates hardware (a logic circuit) that implements this functionality. Such a flow is attractive for two reasons: the higher level of abstraction results in shorter design time and makes hardware design accessible to a larger set of users and the generated hardware does not have to be verified if the flow guarantees correctness. We have created such a correct-by-construction high level synthesis flow. This flow uses an intermediate representation called AHIR[1] which decouples programming language issues from hardware details. The flow is currently implemented as C-to-RTL(VHDL). A circuit generated using this flow can be up-to 100X energy efficient as compared to a processor-based implementation. The AHIR tool-chain continues to be developed and improved. Ongoing work is related to optimizations in memory subsystem and in the mapping of parallel algorithms.

High Performance Analog and Mixed-Signal VLSI Design for Emerging Applications

Faculties Involved: Prof. M. Shojaei Baghini, Prof. D. K. Sharma

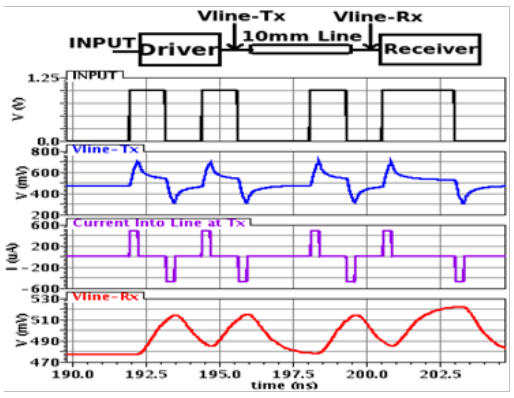
- Emerging applications such as smart personal healthcare, biomedical and sensor applications and power-autonomous systems demand high-performance low-noise conditioning CMOS analog integrated circuits, data converters and special wireless communication modules. Basically interfacing with any sensor requires sophisticated and highly precise analog signal conditioning circuits and particularly with minimum energy consumption for portable (mobile) applications. We design state of the art techniques and novel analog circuits to achieve the best performance for the required functional modules, mostly in CMOS technology. We then make the layout of the design and send it to the foundry. We receive test chips after fabrication and test them [2,3].
- Power management for System-on-Chip (SoC) is another research theme which demands high performance analog VLSI. We work on custom integrated power management modules in nano scale CMOS technologies [4].
- Integrated AC to DC conversion forms a new category of analog and mixed-signal circuits which have been evolved recently for energy harvesting applications. At present we work on the efficient custom integrated circuits for RF energy harvesting. In this context appropriate antennas are required to provide the input to energy harvesting chip. Prof. Girish Kumar contributes to the design and implementation of antennas [5].
- Analog aspects of digital circuits, high-speed data converters (GSamples/s), high resolution, data converters and energy efficient ADCs are other areas of research in high-performance analog and mixed-signal VLSI design [6].

For all research themes, mentioned above, we develop novel circuits and techniques, optimize them and implement them as custom ICs. We submit the designed ICs to the foundries. After receiving fabricated and packaged ICs we test them and then we prototype systems using our own custom ICs.

High Speed Communication Systems

Faculties Involved: Prof. D. K. Sharma, Prof. S. Gupta, Prof. M. Shojaei Baghini

For the past thirty years, the driving force behind semiconductor industry has been the rapid scaling of transistor feature sizes on a chip. This exponential scaling has enabled higher degree of integration and higher frequency of operation. Although the technology node keeps shrinking, the overall chip sizes have been increasing to provide various functions demanded from each chip. With the enhanced speed of logic circuits and chip sizes, speed of on-chip global interconnects has become a critical factor in determining performance of multi-functionality ICs such as System-on-Chips (SoCs) and multi-core processors. Also, with the increased computation speed, demand for very high data-rates in inter-chip communication has also elevated. We, at the VLSI Lab, design novel circuits to enable reliable multi-Giga bits/sec. communication over long on-chip interconnects and off-chip buses at very low energy consumption. There are quite a few research groups across the world actively working on high speed low power signaling schemes for both inter-chip and intra-chip communication.



Most on-chip long (often termed as global) interconnects exhibit a low pass filter like behavior and they can be modeled as distributed RC network. Often the desired data-rates are much higher than 3-dB bandwidth of the wire as shown in Fig. X1. A traditional method to allow high data-rates is to break the interconnect and insert repeaters/buffers before the signal become irrecoverably small. However, the buffers draw a large amount of current from supply, hence consume significantly large power. State of the art on-chip signaling schemes employ equalization circuit in the transmitter and/or receiver (to compensate for high frequency losses) and low voltage swing on the line (to reduce dynamic power consumption CV2f in the line). Recently, we have demonstrated a robust dynamic overdriving current-mode signaling scheme as an alternative to buffer insertion technique. In this scheme, a large current is sourced into or sunk from the line for a short time when input changes, otherwise a small static current is supplied to line (Fig. X2). This effectively amplifies high frequency components of the input. At the receiving end the small voltage swing on the line is amplified to digital logic levels. This technique offers significant improvement in data-rates and energy consumption.

High speed integrated circuits are also being designed for next generation optical communications, with targeted data rates of 40-Gbps, 100-Gbps and beyond. On the transmitter side, high-speed DACs operating at around 20-GS/s are being designed in standard CMOS technology to achieve modulation formats with very high spectral efficiencies. Novel schemes for generating multi-level symbol sequences for testing such DACs and communication links have already been developed. Overall, receiver electronics have become the bottleneck for these links. A completely new approach is being adopted by us at the VLSI lab to achieve integrated circuit receivers for next generation optical transport systems. This approach promises very low power and low cost implementation of receivers for systems.

Memory Subsystems in Multi-Processor System-On-Chip

Faculty Involved: Prof. M. P. Desai

General-purpose processors are heading toward Multi-Core and Many-Core architectures. In such systems, memory is a critical component and often a performance bottleneck. Our work targets modeling and understanding the memory sub-system (at the architectural level) to investigate if good designs or optimizations can be generated in a well defined manner by using knowledge about applications. Towards this goal, the following work has been done:

1. Development of a simulator Memsim for modeling a generic memory subsystem
2. Techniques to identify the performance bottleneck for a given memory configuration running an application and justification of simple performance models that speed up design space exploration [7]
3. Investigation of data placement as one front for optimization of memory systems [8]
4. The ongoing work includes building a simulation framework for realistic models of many-core systems with processors, memory hierarchies and caching, on-chip interconnect networks etc. An important thrust of the ongoing work is to validate hypotheses on actual many-core systems.

General activity of VLSI lab: Chip Design and Testing

Faculties Involved (in alphabetical order): Prof. A. N. Chandorkar, Prof. Shalabh Gupta, Prof. J. Mukherjee, Prof. D. K. Sharma, Prof. M. Shojaei Baghini

At VLSI Lab, we come up with novel circuits, optimize them and implement them on custom ICs. We get the designed ICs fabricated from a commercial foundry in an industry standard CMOS process. The fabricated chips are tested in IC Testing Lab, a part of Characterization Lab-I and WEL Lab at IIT-Bombay.

Designing the chips to prove circuit ideas on Silicon involve many tasks to be completed by designers even after completing the circuit design. For IC design the designers need to prepare layout of the main circuit, extract parasitic resistors and capacitors from the layout, simulate the circuits to ensure that the main circuit meets the desired specs even after including the extracted parasitic resistors and capacitors, design and layout of on-chip test circuits to measure important specs of the main circuit, integration of the complete circuit with the padframe with ESD protection circuits etc. Fig. X3 shows photograph of one of the recently designed chip by us.

For testing of the chips printed circuit board (PC boards) are designed to apply desired inputs and observe the output automatically. Some of the circuits are tested using a probe-station based measurement setup in which a bare die (a die not packaged) is probed.
Some of the recently fabricated (in 180nm CMOS process) and successfully tested ICs are listed below.

5. A Robust, Low Latency and Energy Efficient Signaling Scheme for On-chip Global Interconnects: Sub nanosecond delay of a 10mm long wire has been measured
6. High-speed comparator and offset compensation circuit
7. Signal conditioning circuits employing ultra low-noise ultra low-power INA, rail-to-rail active filter and RLD modules for biomedical and sensor applications
8. Current reference circuits: Current reference with +/- 7% accuracy measured over 50 dice and three different temperatures

These projects are a few examples of the ongoing work at VLSI lab. Other projects include large scale circuit simulators, design of high-performance low-noise signal conditioning ICs, wireless communication interface for healthcare, sensor applications, energy harvesting circuits, design of energy efficient ADCs etc. The lab enjoys good industry support and interaction and has signed MoUs with many global players in the field.

The positive research atmosphere and the general feeling of academic harmony in the lab result in most projects being collaborative in nature. The lab is always open to inquisitive new students who seek to work in the ever-growing field of VLSI. We encourage you to visit our page on the Department website for any details! VLSI lab cherishes good support from the department and institute and hopes for increased assistance in proportion to the results in coming years. ■

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e – Prayog: Virtual Labs (Electronics), IIT Bombay

Compiled by Abhishek Kamath (WEL RA) (On behalf of the entire Virtual Lab team of WEL)

The "Virtual Labs" project was started at the Wadhani Electronics lab in March 2010. It is an initiative of the Ministry of Human Resource Development, Government of India, with an aim to enhance the level of engineering education in the country. The participants include several other IITs and a few other institutes. As IITians, studying here at the Electrical Engineering Department, we are really privileged to have excellent faculty, state of the art amenities and more importantly- 24x7 access to some of the finest labs in the country. Apart from the premier institutes like IITs and a few other colleges, the situation isn't very bright elsewhere. Having visited many colleges in Mumbai earlier and a few colleges across India, as a part of our reach-out initiative, we found this to be true.

We started out by developing learning modules for a couple of courses namely DSP and Digital Design. The DSP module consists of three remotely accessible setups comprising of a DSK6713 kit, a function generator and a DSO - all of which can be controlled remotely. The user can write a program for a DSP operation in either assembly or C and the same can be programmed and executed on the kit. Well, there is nothing virtual about it! The program is physically running on the kit and the user controls the instruments in real-time. Although not originally a part of the Virtual Labs, this was well appreciated by the critics in Delhi.

As part of the digital design module, a low cost CPLD development kit 'Helium' was designed. This was also a detour from the original plan to have a remotely accessible FPGA board like its DSP counterpart. However because of scaling-up issues which are yet to be resolved for the DSP system as well, we felt that the detour was worth trying. And 'Helium' did turn out to be a great teaching tool. Currently around 1400 such boards are being used by approximately 200 engineering colleges across the country. It also garnered a lot of positive feedback from the reviewers although it again defied the 'virtual' philosophy! It happens to be the perfect complement in teaching a first course on Digital Design and HDL. We are in the process of designing an FPGA based board on the same lines. The remotely accessible FPGA system is also close to completion.

Each of the above two modules are extensively supported by requisite theory, sample programs, tutorials on using the systems and a good number of exercise problems for the interested user. We conducted numerous workshops to reach out to the masses for which this project is targeted at. The feedback received from the teachers and students alike has been quite encouraging.

So you might be thinking what is "virtual" about the project? Well, nothing you have read so far! In order to have something that gives the feel of a lab without actually being present, we finally decided to get 'virtual'. A couple of labs based only upon simulation and animations are now ready for use. The prime focus is on 'Electronics Device and Circuits' and 'Signals and Systems'. Experiments can now be performed in a manner that it gives the feel of a real lab without the involvement of any equipment whatsoever. Java applets are used to demonstrate the basic concepts of each topic in a very interactive and illustrative way. This has also been appreciated by both students and teachers thus ensuring that we have been successful in implementing what we had in mind while staring off.

We would like to know your opinion as well. So get virtual and visit *http://59.181.142.81/* ■

The OSCAR Project

Phani Swathi, Project Associate, OSCAR

Each of us have had trouble at some or the other time in explaining or understanding concepts in science or engineering and we have all thought – "I wish I had a model or a movie to explain and understand this!" Now here is an opportunity for you to make animations explaining scientific and technical concepts and be paid for it too! OSCAR, which stands for Open Source Courseware Animations Repository, is a combined initiative by the various departments of IIT Bombay to create animations which aim to explain basic and advanced concepts in Science and Technology in a sequential and structured manner. This makes all those last minute dodge games with circuit theorems and signal transforms a wee bit easier!

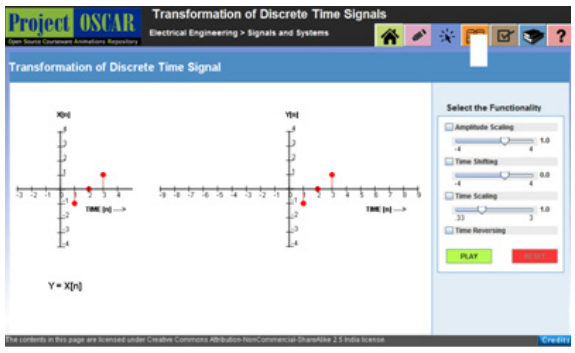
The project is open-source and available for free to all internet users under the Creative Commons License Attribution-Non commercial Share Alike 2.5. Project OSCAR recently won the 'Best Open Source Initiative' at eINDIA 2008, one of the largest Information and Communication Technology conferences in the country!

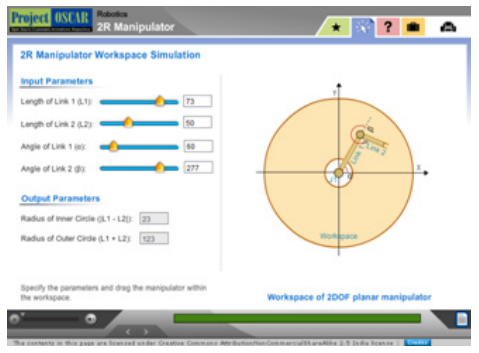
Project OSCAR was conceptualized by Prof Sridhar Iyer of CSE dept, IIT Bombay, who is also the current Principal Investigator of the project. At the EE department, OSCAR initiative is taken up by Prof. Saravanan Vijaykumaran, whose team develops animations for error correcting codes and related communication systems topics. Mrs. C. Vijaylakshmi at IIT Bombay, a co-investigator of this project, manages the implementation of the various front-end and back-end systems. Project OSCAR evolved out of the xNET Project, which served as a pilot study with focus on creating animations for concepts/protocols in computer networking.

The animations in Project OSCAR include concepts ranging from high school subjects to advanced topics in many areas. Each animation is typically a Java Applet that focuses on one concept and provides the following through a platform-independent, web-interface:

- A brief description of the concept, including relevant references.
- An in-built animation, to explain the concept in detail.
- An interactive animation, wherein the user defines the parameters.
- A self-assessment questionnaire for the user to test his understanding of the concept.
- Earn a reasonable honorarium for your valuable conference.
- Downloading of the source code, for "local" use/study/modification.

The interactive nature of these Java applets is the key difference from other types of animation, such as openoffice, powerpoint, flash etc. Perhaps, the best part about OSCAR is the entire phenomenon of give-and-take that it promotes. It not only provides the animations, but also the opportunity for anyone to be the designer of animations and be paid for it!





So it is a two-sided learning game!

Participation in OSCAR is in one of the three roles:

1. **Proposer**: One who proposes the concept, design and animation flow. Generally this role is for course instructor and industry professionals.
2. **Developer**: One who develops the JAVA applet according to the guidelines provided by the proposer. Generally meant for students who are comfortable with JAVA applet design in consultancy with the proposer.
3. **Reviewer**: A domain specialist who reviews the submitted animations and suggests improvements.

The entire flowchart for the process may be viewed on the Oscar website. In order to register for OSCAR, please visit the website – *http://oscar.iitb.ac.in*

The OSCAR project has been funded by the Development Gateway Foundation and Open Source Software Resource Center in the past. Presently, the project is funded by Tata Teleservices IITB Center for Excellence. OSCAR also enjoys continued support by the Ministry of Human Resource Development, Govt. of India.

Currently the project has 218 registered developers, 248 registered proposers and thousands of animations and 3-D models for explaining a diverse variety of concepts. Yet, there is room for many more to join the group and add to the repository. Students are encouraged to visit the project website for any details and also provide feedback on their experience with the animations.

Learn things, the OSCAR way! ■

Compiled by: Abhimitra Meka (1st year M.Tech.-ES)

Sensing and Cancellation of Tremors in Surgeon's Hands during Microsurgery

By Nikunj Bhagat. The author is an alumnus of Department of Electrical Engineering, IIT Bombay (Batch of 2011, M.Tech. (Control and Computing)) and is currently working as a Researcher in Department of Robotics Engineering, Daegu Gyeongbuk Institute of Science & Technology (DGIST), Daegu, Republic of Korea. This article is a brief overview of his M.Tech. Thesis completed under the guidance of Prof. Debraj Chakraborty (Electrical Engineering Department) and Prof. P. Gandhi (Mechanical Engineering Department)

Introduction

Microsurgical operations are performed on small and delicate organs of the body like inner ear, retina, nerves, etc. With the aid of a compound microscope and specialized instruments the surgeo operates on tissues as thin as 20 µm [1]. Therefore human hand tremors, which are equal in magnitude to the tissue being operated, are a major hindrance to the precision of surgeons. Tremors are involuntary motions and their suppression will significantly improve the safety, accuracy and effectiveness of the microsurgical operations. Passive techniques for suppressing tremors try to reduce surgeon's fatigue and increase his/her comfort using arm and wrist supports [2]. We propose a novel approach for sensing and canceling hand tremors during microsurgery using an active glove. A glove device embedded with sensors and actuators will be worn by the surgeon while operating. By measuring the finger tip deflection the actuators will produce the required compensatory forces on the fingers, to cancel out the resultant tremors at the instrument tip.

The work performed as part of the Master's Thesis for this project had two main objectives. First, to design an integrated hand glove-based sensing device for measuring and real-time plotting of finger tip displacements in 3D. Second, the project demonstrated the design and implementation of a controller for 1D tremor cancellation, when a person is holding an instrument and imitating surgical movements. This article will describe the glove-based tremor measurement device. For details of tremor cancellation and further information about the project, kindly refer to the author's web page (*http://surgical.dgist.ac.kr/nbhagat*).

System Description

A 6 degrees of freedom (DOF) inertial sensing module consisting of a triaxial accelerometer and a triaxial rate gyroscope was designed for the project. This module was attached to the finger tip of a person to record tremor signals. The measurements were processed by the microcontroller board to calculate the finger tip orientation and displacement in 3D. The block diagram of the complete system designed for tremor measurement is shown in Fig. 1.

An accelerometer measures the net acceleration acting on the body, which is contributed by the body's motion and gravity acting on it. In order to measure the proper or real acceleration acting on the device due to finger tip deflections, the component of gravity in the measurements must be canceled. As seen in Fig. 1, the accelerometer and gyroscope measurements (ax, ay, az) and (p,q, r) respectively, are combined using complementary filters to measure the orientation or Euler angles (Φ, Θ, Θ) of the body. This information is then used to apply coordinate transformation to the measured accelerations and subtract the gravity component. This is followed by double integration

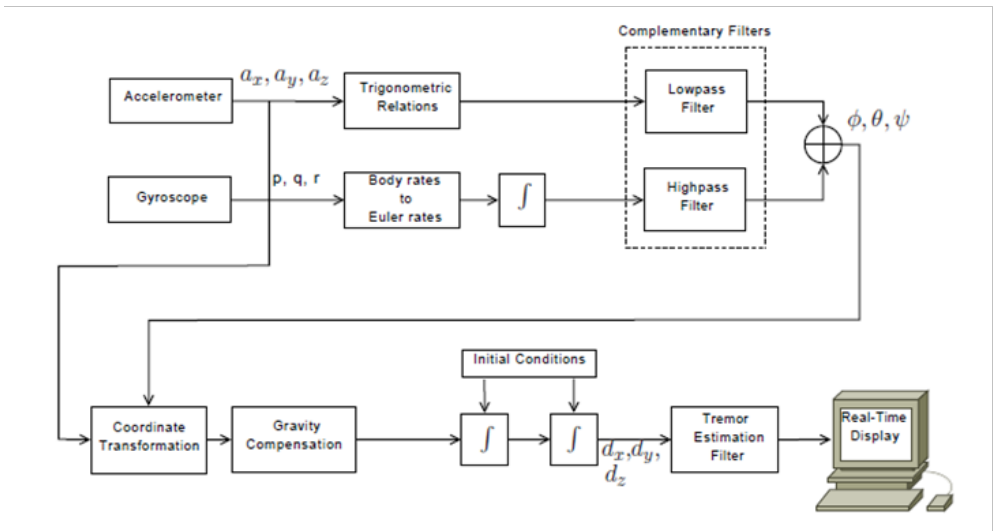


Figure 1: Block diagram of glove-based tremor measurement device

Sensing and Cancellation of Tremors in Surgeon's Hands during Microsurgery (Cont. from Page 3)

of the net acceleration, assuming zero initial conditions, to obtain the finger tip deflection in 3D space (dx, dy, dz).

A prototype board for the tremor measurement device was designed and fabricated. The prototype board contains two boards, namely the sensor board and the processor board. The sensor board consisting of inertial sensors (accelerometer BMA180 and gyroscope ITG-3200) is mounted on the finger tip and could be easily attached to the processor board using Flat Flexible Cables (FFC).

At the heart of the processor board is dsPIC33F Digital Signal Controller from Microchip, which is responsible for reading data from the sensor, calculating finger tip orientation and displacement, and communicating with the computer for data logging and real-time display of tremors.

Results

The accuracy of orientation and displacement calculation algorithms was determined by mountng the prototype device on an experimental setup. Along with the prototype, optical angle encoders and a commercial 9 DOF inertial measurement unit (IMU) 3DM-GX2 were also mounted on the setup. A sample of the roll angle (Φ) measurement obtained using the experimental setup is shown in Fig. 2. The mean error for roll angle estimation using the prototype, for complementary filter cutoff frequencies of 1 Hz and 2 Hz, were calculated to be −0.47° with a standard deviation of 2.14° and 3.2° respectively. These measurements were further used by the microcontroller to calculate the hand tremors. A snapshot of the processor and sensor boards mounted on the hand for measuring tremors is shown in Fig. 3. In the background, a real-time plot of the measurements using the graphical interface designed for the project is shown.

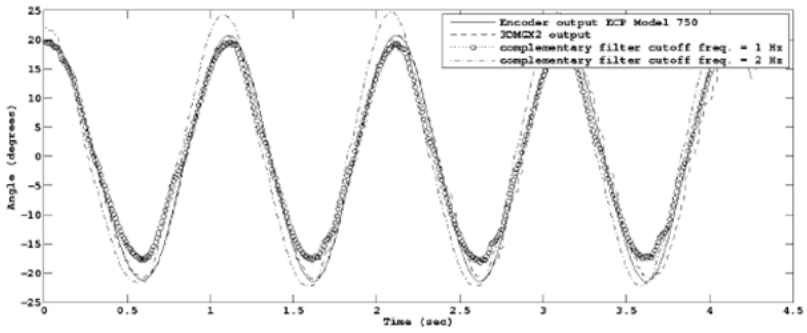


Figure 2: Comparison of roll angle measurement using prototype, angle encoders and 3DM-GX2

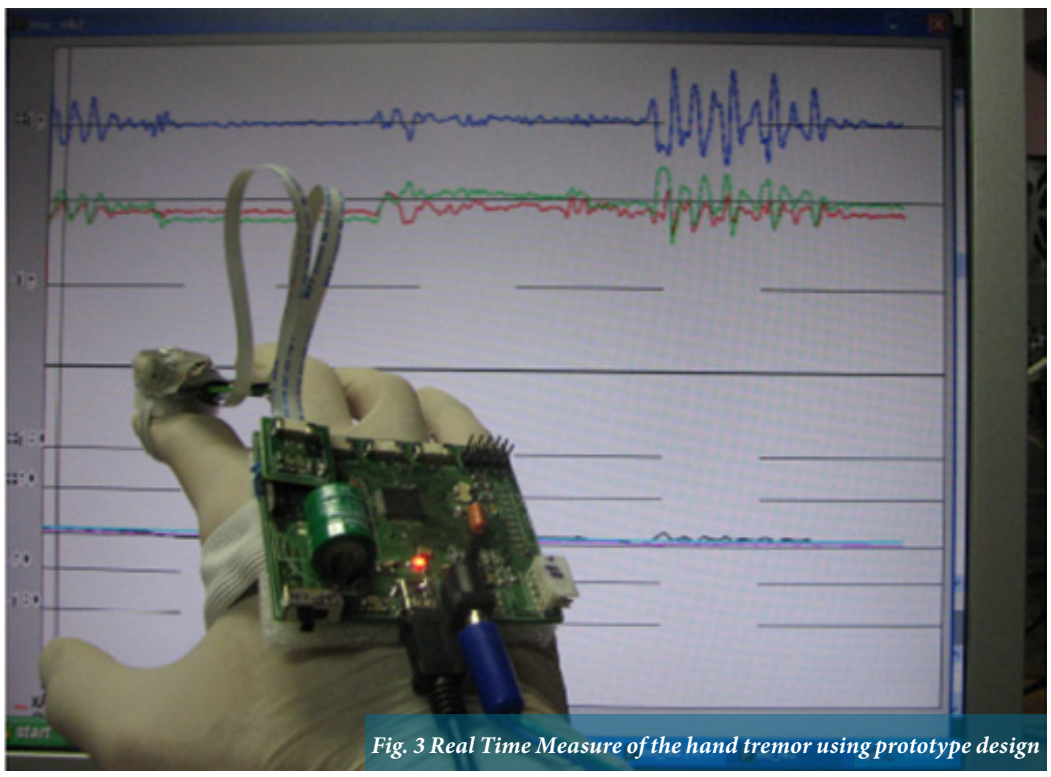


Fig. 3 Real Time Measure of the hand tremor using prototype design

Conclusion and Future work

This article presented the measurement of hand tremors using inertial sensors in a glove-based device. Presently, we are able to calculate only relative and not absolute finger tip displacement due to the unavailability of initial conditions when performing integration of the measured acceleration. The future work will explore the calculation of absolute displacement. A major obstacle in the implementation of glove-based tremor cancellation is the unavailability of commercial flexible actuators. Efforts are currently underway to design in-house electro active polymer-based and pneumatic balloon actuators for tremor cancellation. ■

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Next Generation Wireless Networks: Research Challenges and Opportunities

Prof. Abhay Karandikar, Sanjay Kumar (M.Tech.), Somya Sharma, Dhanashree Deval Parakh (Research Engineers/Project Staff)

Global Scenario

Today there are a plethora of services that are causing Internet traffic to grow by 50% every year. Moreover, nations are become increasingly aware of Intellectual Property Rights (IPR) reserves and are using them to position their trade policy. A good example of this is China, which has pushed its IPR in major 3G/4G standards. With increasing data rates, wireless broadband in mobile phones has evolved from TDMA (Time Division Multiple Access) – based GSM (Global System for Mobile Communications)/EDGE (Enhanced Data rate for GSM Evolution) and WCDMA (Wideband Code Division Multiple Access)/EVDO (Evolution Data Optimized) (2G) to HSDPA (High Speed Downlink Packet Access), HSPA (High Speed Packet Access) (3G) to the more recent, LTE (Long Term Evolution), which can be categorized as 3.5G. Over time, balance of IPR has been shifting; today 40% of the essential patents in LTE are from Asia.

The next generation wireless, IMT-A (Internet Mobile Telecommunications Advanced) (4G) is currently in its specification phase.

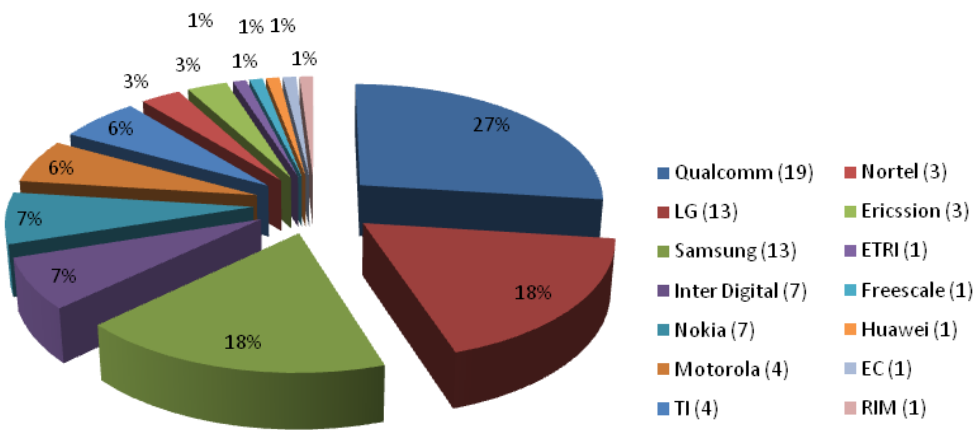
Indian Scenario

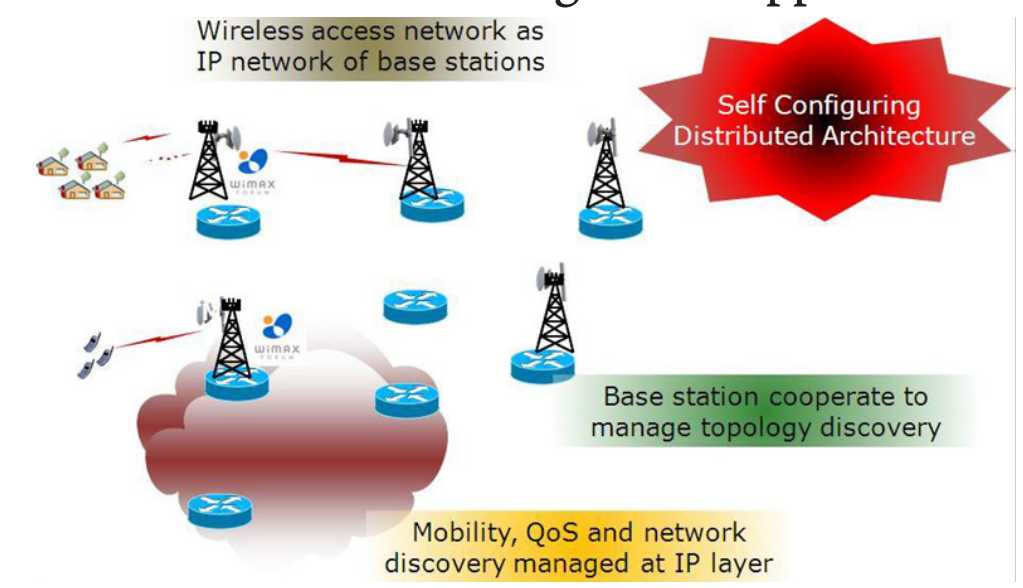
With more than 700 million cell phone subscribers, India is the second largest Telecom market in the world, next only to China. Despite this, most of the technologies deployed in India are imported, making it the second largest import after Oil, resulting in high outflow of foreign currency. Besides, India is the only country among the top Telecom markets devoid of any umbrella body focusing on standards. As a result, India's contributions to next generation wireless technology standards are marginal. With very low Broadband penetration, we have only 60% geographical coverage in India. This number is even lower for villages (25%). Thus, Indian scenario is dismal on more than one count. These issues make improving Indian scene a big challenge and provide ample opportunities for research.

Our contribution: TICET (TTSL – IIT Bombay Center for Excellence in Telecom)

As part of a major initiative taken by Department of Telecom, Ministry of Communications and Information Technology, Govt. of India, Telecom Centers of Excellence have been set up in IIT Bombay, Delhi, Kanpur, Kharagpur, Madras, IISc Bangalore and IIM Ahmedabad in a public-private partnership mode. As part of this initiative, Tata Teleservices has sponsored TTSL-IIT Bombay Center for Excellence in Telecom (TICET) as a major R&D initiative in IIT Bombay in next generation wireless telecom technologies. The center focuses on state-of-the-art research in telecom relevant to Indian service providers in general and TTSL in particular with special emphasis on rural wireless applications and connectivity. The center is being coordinated by Prof. Abhay Karandikar of IIT Bombay and Mr. Sushil Prakash of TTSL and assisted by a team of IIT Bombay faculty members, researchers, students and TTSL managers and engineers.

As part of an initiative to influence international standards to align with Indian requirements, researchers from IIT Bombay have been participating in 4G standardization efforts and have made 13 contributions to the international standard (IEEE 802.16m and IEEE 802.1). IEEE 802.16m in fact, was a BTP by Prateek Kapadia, Gauri Joshi and B Srinadh under Prof. Abhay Karandikar and suggested changes in Bandwidth Request procedure in wireless uplink scheduling. The center has filed 2 key patents in the area of Quality of Service and coexistence





of 4G standards with other wireless networks. The center is also a part of ITU (International Telecommunication Union)'s registered evaluators of 4G (IMT-A) standard. Participation in international standards is envisaged to play an important role in catalyzing telecom manufacturing in India.

Apart from contributing to international standards, we also identified some of the challenges to bridge the Digital Divide in India and the technological solutions that can potentially revolutionize broadband penetration. TICET recognizes that the next wave of mobile revolution will come not only from 3G/4G deployments but also an all inclusive growth in rural telecom deployment which is a big but largely untapped market. It has been well known that one of the major hurdles towards progress of network is non availability of indigenous cost effective backhaul. We are focusing on developing an innovative solution for cellular backhaul based on a modified optimized version of long distance WiFi technology.

Present generation broadband wireless systems are hierarchical - wireless access networks in the form of base stations connect to the Internet through 'packet core networks' (for example Evolved Packet Core in 3GPP). Since the Internet is only at the 'core', management of the access links is done by the radio resource management features. Thus, functions like radio handovers and QoS are managed on the access link layer; network discovery and topology are managed by protocols running between the access and core; and other functions like attachment to the IP network are managed at the core. This leads to a heavy link layer and complex interworking between the access and core. This is much unlike the present generation wired networks, where the network intelligence is in IP layer protocols - for example, Dynamic Host Configuration Protocol (DHCP) for network attachment, Mobile IP for mobility, and IntServ/DiffServ for QoS. The performance of these functions in the network layer leads to a lightweight link layer protocol, and leads to easy interoperability between different network domains and technologies.

An easily configurable and manageable architecture like the existing Ethernet technology, coupled with seamless integration with the Internet cloud will enable low cost next generation wireless access in countries like India. On the RF / physical layer front, TICET has made significant contributions in the area of enabling coexistence of BWA (Broadband Wireless Association) technologies with other wireless technologies (such as WiFi) which operate in neighbouring frequency bands and hence have the potential to degrade performance of BWA systems. This is important for India since operators typically design their network with low link budget margins to cope with the large number of users, hence making link quality more susceptible to such interference. Moving forward as popularity of technologies such as WiFi grows, such co-existence mechanisms will play a critical role in ensuring quality of service to end users.

This is the first time that Indian IPRs and requirements are being presented at International forums. So far, Indian presence in standards was negligible, but with TICET's efforts, this has become possible now. ■

Compiled by Alankar Jain, 3rd year, DD-CSP

High Dynamic Range Imaging – A Technical Overview

Shanmuganathan Raman is currently a Post-doctoral Research Associate at the Indian Institute of Science (IISc), Bangalore. He obtained his M.Tech. and Ph.D. both from Indian Institute of Technology (IIT) Bombay. He was awarded Microsoft Research India PhD Fellowship for the year 2007. Author's mail Id - *shanmuganathan.raman@gmail.com*

Due to the digital revolution, analog cameras are rarely used these days. Digital cameras provide us sophistication in the sense that one can review the shot picture immediately apart from making any changes to the picture. Cost and expertise required for one to use digital cameras is minimal. These benefits of digital cameras over the analog cameras have made them ubiquitous in imaging. Digital imaging has become the most widely used term at present and no one bothers much about analog imaging.

Real world scenes have a range of brightness levels so high that common digital capture devices are unable to capture the entire range. This drawback is mainly due to the restriction of capacity of the each sensor element present in the camera sensor array. Analog cameras can however capture higher range of brightness levels than common digital cameras, as the brightness levels are recorded in a continuous form through burning of oxides in the film.

There are digital cameras which can capture High Dynamic Range (HDR) scene information in a single snapshot such as Spheron VR camera. However, such cameras are very expensive at present. The challenge is to enable common Low Dynamic Range (LDR) digital cameras to capture the HDR information. We shall now look at the new imaging paradigm called HDR imaging which enables one to capture higher dynamic range even with the common LDR capture devices. The advantage with such an approach is that the cost is less compared to re-designing the imaging sensor.

A real world scene which has both brightly and poorly illuminated regions is said to be an HDR scene. If we take multiple images of the scene using a digital camera by changing the exposure times, we would be able to capture all the details of the scene. Auto-Exposure Bracketing (AEB) feature in common digital cameras lets one capture this sequence. However, the details of the scene are now distributed across all these multi-exposure images (See Figure 1 (a-i)). We need to appropriately weigh the intensity values of these images to capture all the details in a single image. This process requires us to remove any non-linearity introduced by the digital camera before weighing the intensity values.

Many commercial software products perform this task. Some of them are HDRsoft Photomatix, pfstools and Adobe Photoshop (CS2 onwards). Even recent releases of MATLAB have functions such as hdrread, hdrwrite, makehdr, and tonemap to achieve basic HDR image operations. HDR images are encoded in formats such as Open EXR (.exr) and Radiance RGBE (.hdr) which store a floating point value at each pixel location. The generated HDR image is then subjected to a process called tone mapping for display in display devices which can understand only LDR content. The LDR image corresponding to the multi-exposure images in Figure 1 (a-i) is shown in Figure 2.

Problem in multi-exposure image capture arises when one needs to capture a dynamic scene. Real world scenes are dynamic (objects in the scene are in motion). Even an expert photographer does not have any control over the movement of objects in the scene while capturing multi-exposure images. If the scene changes are not detected in the multi-exposure images, the final HDR image will have artifacts called ghosts. Several de-ghosting algorithms have been developed which eliminate such artifacts due to motion in the scene.

Fig.2

The real challenge for HDR imaging in future is the development of fast algorithms which can produce artifact-free HDR image corresponding to both static and dynamic scenes. Real time tone mapping operators are also a challenge which can then enable HDR images to be visualized in common LDR displays. Inverse tone mapping techniques, which enable existing LDR content to be visualized on HDR displays, are also of much interest to the research community. ■

Fig. 1: multi-exposure sub-images (Courtesy: Erik Reinhard, University of Bristol)
a. to i. from left to right

A look at various events organised by Electrical Engineering Students' Association (EESA) in Autumn Semester 2011

Compiled by Sabareesh Nikhil and Sampath Satti (2nd year – B.Tech.)

Traditional Day

Tees and shorts, most likely unwashed since many days, went for a toss, as kurtas, refreshingly non smelly, took centerstage. The electrical engineering department of IIT Bombay was at it's traditional best. The air was replete with enthusiasm, curiosity, courtesy the freshmen, and nostalgia for the fourthies and the fifthies. This is one special day when the many different islands in our department are bridged.

As has become tradition, the trad day was held on the occasion of teachers' day. It couldn't have been held on a better suited day, with our rich tradition and the people who pass it down generations, being cherished together. Our HOD, Prof DK Sharma, cut the cake. Professors AN Chandorkar and Maryam ma'am were also present for the ceremony. The magical cake disappearance act took place this year too, with it's lifetime measured at 8 seconds. The Electrical Engineering Students Association pulled out all stops to ensure that the event was a memorable one.

It was then time for the batch photographs, which are dearly treasured by everyone. The enthusiastic crowd kept surging forward, every person trying to get into the first row. (The poor photographer was literally harangued for photographs. His ambiguous facial expressions were not helping either. People didn't understand, whether the photo was taken or not.)

But the image that'll remain with me forever was that of Maryam Ma'am, who stood in the front of the crowd, plugging in her ears to the raucous cheers, with a smile on her face. That for me, symbolizes the relationship between 2 generations that are so different, yet have so many things in common. After 30 minutes, the GG foyer was back to it's normal state, with guys in shorts, sporting unkempt hair, waiting for their class to begin.

Department trip to Malshej Ghat

Buses buzzed with activity, and emotions ran high as the Department of Electrical Engineering geared up to cross yet another milestone. Only, this one read, 'One kilometre to Malshej ghat'. An electrified ambience pursued all 200 prospective electrical engineers of us, and our shrill cries of sheer exhilaration cut through the still morning air. Off we were!

The first rays of the morning sun saw us - the very IITians usually tightly tucked up in bed, unwilling to be woken up at that unearthly hour - bubbling with enthusiasm and boarding the buses in noisy packs. The Department came alive. Yes, we were all looking forward to a rendezvous with Enchantress Nature, to delve into a whole new world of adventure miles away from that hub of bustling activity we call IIT, an excuse to spend some quality time with friends. Transistors slowly gave way to trees, and enveloped in lush greenery, we could hardly have enjoyed more, what with hybrid games being played, each more out-of-the-way, and consequently more occupying, than the previous. We gave vent to our knack of being lukkha, and songs and jokes charmed every little hint of pressure out of us.

Five hours of fun and frolic, and the Ghat loomed in front of us. Every inch of us was tingling to scale it. Backpacks on, we embarked on a three-hour trek. Freshie enthu notwithstanding, nimble-footed seniors led the way up a well-worn trail, while the more adventurous and simply inquisitive raced off along various shepherd trails into wild shrubbery.

Soon, backpacks became lighter; water in our bottles now coursed through veins, and our thirst quenched, we resumed skipping from one rock to another on lighter feet. Drenched in sweat and exhausted, we nevertheless wound our way up the hill, our spirits unwearied. And photographs – loads of them: all saw us grinning cheek to cheek, our weariness masked by elation.

It took our rumbling stomachs to remind us that we had to return. An enjoyable meal of some very savoury Veg. Pulao (EESA, thank you!) ensured that we enjoyed the return journey just as much. The climax turned out to be eventful indeed, with a group of B. Tech sophies requiring the help of a local to come down, as the rest of us spent some time remembering Mallory and Irvine. A bath at an adjoining dam, and we called it a day when one of us spotted a shed snakeskin nearby. The journey to IIT took little time, or so we felt, and spent physically but re-energised mentally, the Department was back to where it belongs.

ECSP (Electronics Club Summer Projects)

Another year, and another set of electronics club summer projects were professionally coordinated and successfully completed by the Electronics Club of IIT Bombay, with support from the Electrical Engineering Department. The projects saw around 20 groups of students managing to finish their projects in the given timeline, with great looking bots, and solid documentation to go with. Students from all departments participated. The ideas were as diverse, some (read lazy) wanting to make life easier by making wireless switching systems, others for fun, like Laser pong and an IR harp, while others with a view to help handicapped like, the hand input gloves. The common uniting factor was the creativity of the ideas behind the project, and the enthusiasm shown by the students, staying back in the institute for practically their entire summer vacation, some after their first year itself.

A refreshing change observed this year was the compulsion of documentation of the projects on a real time basis from the teams. This gave a reality check to teams, and also, making the code open source, allows further groups of students to use a certain projects as customizable module in their larger project. All the documented projects can be found at: http://stab-iitb.org/wiki/ECSP_Home

Here's a brief overview of one of the projects, in words of the students involved!

Project - IR Harp
Team - Sumeet Fefar, Ashwin Kachhara, Prakhar Khandelwal, Samitinjay Patil, Nachiket Deo
Mentor - Ranveer

We made an IR harp last summer. A harp sounds pretty primitive, but trust us, we practically had to use every single fundae we got in EE112. The basic project was to replace the strings of the harp with an IR emitter sensor pair. A gap in the output values caused by a motion of the hand, say would be recorded and output as sound.

As every electronics project goes without saying, we faced many difficulties, and solutions involved opening up a casio keyboard, and countless hours in the WEL, playing around with the outputs on the oscilloscope. The enthusiasm levels were so high, that we almost finished the project on our own.

The aim of our project was not just to build a functioning one, but build it with the simplest items available. We used R-2R ladders for DAC conversions, and opamp circuits for filtering. Doing all these very recently in EE112, was a boon. The ECSP ensured that we would never forget the basics of electronics. Ever.

Lots of seniors, who had done similar projects last year, had stepped in to mentor the teams this year. With such a tried and trusted method of passing down knowledge (read fundae), and the continued support from the Department, this initiative is bound to go many more places in the future.

Department Freshie Orientation

Written by Yamini Bansal, Compiled by Sharath Reddy

in-tro (in- troh) Noun
1. *A formal presentation of one person to another.*
2. *Means by which seniors at IITB exercise dominance over their juniors under the name of breaking the ice between the two.*
3. *A practice that is highly resented or feared by many in the socially weaker section, the freshies, in IIT.*

It was a seemingly ordinary day. The mess table was filled, as always, with laughter and conversation. Except, the "maggu elec junta" looked as they do when they have a paper to give – happy, excited and apprehensive at the same time. You'd find one of them jump up at the sight of a senior and desperately enquire about something. Oh well, this was the day of "Elec Freshies Got Talent". Formally called the Electrical Engineering Department Freshmen Orientation. Being the first of all department orientations, it had an added element of suspense to it.

All the freshies were asked to assemble in the seminar hall in the evening. A small video showing the happy electrical family preceded the real show. No, not just Resistors, capacitors, and transformers.

Intros ! The freshies were called on stage one by one and asked to introduce themselves- strictly in Hindi. Apart from the usual questions about AIR and Rollbaap/ma, they were asked to impress, to entertain. While quite a few charmed the crowd with their baritone, some chose to go a step further and scorch the stage with their moves. One freshie also drew her ilk on the board. The plethora of their talents extended to acting. The evening also saw mimicry and attempts at a ramp-walk. While the "introphobic" wanted the ordeal to end, the others enjoyed the rather informal show. The evening was concluded by cutting a cake.

This orientation that was aimed at making the freshies feel welcome to the department definitely found a place in the memories of all. ■

"Know Thy Turf" – HPC Lab

Compiled by Alankar Jain (3rd year DD-CSP)

Located on the 2nd floor of EE Annex, High Performance Computing Lab (HPC Lab) was established in 2008 with initial support from Tata Consultancy Services Ltd. Since then, it is being convened by Prof. Sachin Patkar.

The primary goal of researchers at HPC lab is to research to address future needs of high-end parallel computing and to develop high-performance and practical solutions to newly evolved problems in system design and contribute to the needs of both scientific and engineering community.

Multiple resources of all kinds such as high – end computers, NVIDIA Graphics Processing Unit for Parallel Processing, 9th and 10th generation GeForce cards and various types of FPGA boards are available to researchers to carry out work related to high – performance computing.

HPC lab has undertaken many projects in collaboration with Naval Research Board (circuit simulation, multimedia computing and general scientific computing), Computational Research labs, Pune (supercomputing), Tata Consultancy Services Ltd. (high performance error-correction codes), ISRO (Indian Space Research Organization), Indo – German Research collaboration (supported by Department of Science and Technology, India and German Research Foundation). Many of these projects have been completed while some others are still going on. Many other projects are being investigated by Prof. Sachin Patkar, Prof. H. Narayanan, Prof. D.K. Sharma, Prof. Saravanan Vijayakumaran, Prof. V. Rajababu, Prof. Madhav P. Desai, Dr. Gaurav Trivedi and other doctoral and graduate students.

Around 5 patents have been filed so far, out of which 1 has been published ("A system and method for emulating a logic circuit design using programmable logic devices", Patent Application No. 211/MUM/2005, Published 2005-06-04, Filed 2005-02-05, United States Patent Application Pub. No. US 2006/0247909 A1, Pub. Date Nov. 2, 2006. Madhav P. Desai, and Sachin B. Patkar(IITB) and Himanshu Sharma, Mitra Purandare(Powai Labs). Apart from these, HPC lab has been publishing numerous journal articles, conference articles, handbook chapters and technical reports.

For more information on the lab and its activities, visit: *http://www.ee.iitb.ac.in/~hpc/* ■

Introducing Smart Grids in India

Compiled by Preeti.G on behalf of V S K Murthy Balijepalli (a Research Scholar under Prof. S A Khaparde)

Remember Shahrukh generating power for his village in 'Swades'?! It's time again, for India to analyze its power generation and distribution mechanisms to meet the huge power requirement of today. The current scenario is very bleak. Power thefts are common and are difficult to track. Distribution systems have grown in an unplanned manner resulting in high technical and commercial losses in addition to delivering poor quality of power. The current power generation capacity in India is around 175W/hr while the requirement is way more than this (300W/hr). The identified way to completely overcome these problems is by reducing demand through electricity grid intelligence, which requires advanced control and communication technologies integrated with the utility network, thus providing the requirements of "Smart Grid".

A "Smart Grid" is a concept for transforming the nation's electric power grid by using advanced communications, auto-mated controls and other forms of information technology.
So, in what ways is a smart grid really smart?
How will it change the life of a common man and of the entire nation as a whole?

Let's have a look at two basic changes that smart grids will introduce:
Decentralized Power Generation and Distribution
In the current scenario, electricity is generated by various power plants and then reaches the end consumer after passing through a long chain of distribution and utility networks. Obviously, there are losses involved while transmitting power over long distances. The smart grid concept aims to enable power generation at every household. The technology used can be any – solar being the most common. The Jawaharlal Nehru Solar Mission aims to establish India as a global leader in solar energy by 2020. This will involve implanting solar panels in every household. So, for the first time the consumers themselves will be involved in generation and distribution of power. The Government also plans to give subsidies to people who would generate a fixed quantity of power.

Real Time Price Fixing: Smart grids will also enable dynamic real time power pricing based on the demand and supply, as against the current fixed and rigid power pricing scheme.

The changes involved are plenty. It is not practical to replace the current system with smart grids, in one single shot. These changes have to be brought about in phases, the technical details of which have been proposed by us and accepted by the Government of India, to be in the agenda of next 5-year plan. For more information, log on to *www.desismartgrid.com*! ■

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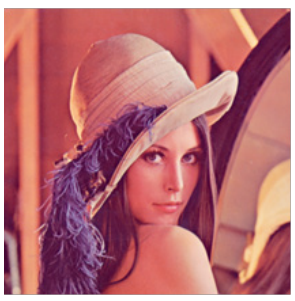
The Story of Lena

Compiled by Abhimitra Meka (1st year M.Tech -ES)



For decades now, the 'Lena Image' has held a special place in the Image Processing academic community. The most widely used image by researchers for testing compression schemes and image enhancement techniques, the popularity of this image is evident from the fact that almost every student of engineering is familiar with this image either from some obscure research paper or a text book. The source of such an extremely popular image is a startling story in itself!

The 'Lena Image' comes from the centrefold of the November 1972 issue of a ragingly popular adult magazine! The image is that of a model by the name Lena Soderberg originally from Sweden. Lena herself did not know about the popularity of her image till 1988. Later, as an invited guest to the 50th anniversary IS&T conference in Boston held in May 1997, she was proclaimed as the 'First Lady of the Internet'!

The first digitized 'Lena image' was a result of a hurried search for a test image for a conference paper, way back in 1973 at the University of South California's Signal and Image Processing Institute. Then an Assistant Professor, Alexander Sawchuck, along with a grad student and the lab manager, digitized the top one-third of this photograph using a Muirhead wirephoto scanner integrated through an ADC to a HP 2100 minicomputer, and created history! Understandably, the image of an attractive young woman, the likes of which very few students and researchers get to see in their own daily lives, is appealing and thus the image continues to command fervent adoration in the image processing community even today. Technically speaking, a large dynamic range, richness of edges and depth features, good amount of defocus and contrast are amongst the characteristics that make it a good all-purpose test image!

Over the years, the image has been a major topic of controversy. So much so, that the editors of prestigious publications such as SPIE Journal of Optical Engineering and IEEE transactions on Image Processing have had to publish editorials justifying the continued usage of this image. While many groups have requested for a ban on its use, the editors clarify that the image processing scientists, especially women, have never filed such complaints but instead have ridiculed the controversy itself!

A noteworthy fact is that the November 1972 issue of that particular adult magazine sold the highest number of copies in its history – a whopping 7,161,561 copies! Many 'Playful' engineers out there, it appears! For further read, one can visit Dr. Ruth's page at *www.cs.cmu.edu/~chuck/lennapg/lenna.shtml* ■

"Ab Ham Sabhi Bahut Haste Hain"

By Aditya Shankar (1st year, B.Tech.)

Indeed. But laughter is an understatement. It's rather a bunch of teenaged specimens from some psychoanalysis lab bursting out in a hysteric outpouring of insane emotions. Quite a heavy line, but trust me the laughter is more "khatarnaak" than this.

But it's good that we are laughing, at least it takes away the tension associated with the EE111 assignments. EE111 Assignments are epic, the first stage involves people slogging in their respective rooms to understanding what is being asked, after 10 hours or so, the second stage commences with everyone shifting their bases to one odd room chosen totally randomly (Yes, we do put in those 6 hours for IC 102) and indulge in group studies. It doesn't take really long for the third stage to begin; actually there is no predefined boundary. The group discussions proceed to a babel of confused frustrated minds, and I mean that quite literally, visit a EE freshie wing the night before the submission and you out to get the feel of a fish market. But by the end of the third stage, we have completed what was asked for, the assignment, and realise the power of unity. We're left with a feeling of slogging our hindbacks off to get the assignment done. Next day we go to the quiz just to realise to our dismay that we know nothing at all. - "Bhool gaya hoon sab kuchh, yaad nahi hai ab kuchh."

"Man, its too risky to go this way" – exclaims a friend while we enter the GG building, still sceptical on the probability of getting pooped upon. But even this exclamation has a sense of overjoyed belongingness associated with it; I mean who doesn't enjoy birds having a nice time pooping on them. After the ordeal of crossing successfully, we bask in its glory. The Department of electrical engineering, that's what sets us apart (I mean, which department has birds welcoming them with a white carpet!?), and synchronises us in a harmony of individual minds flocking together.

"Mera Naam Aditya hai, aur main Vidyut abhiyantriki ka vidyarthi hoon" (my name is Aditya and I am a student of Electrical Engineering) - in chaste Hindi. And so began our introduction with seniors of the department. I had got the the upper shelf, cleverly christened Kashmir, in the small pigeon hole rooms of H2 and with my introduction began the cascade of falling intro dominoes. With random sentences and their derivations, the unique IITB lingo and the regular Gali fights, the introduction was fun for everyone. It really helped do one thing for sure - open up a communication corridor with our seniors.

With the first semester nearing its end, I feel as new as I was five months ago, yet there is a sense of complacence which sets in with every passing day. A sense of being at home. Thank you, IIT Bombay. ■

Eclectical Engineering

By Neeraj Gopal (2nd year, B.Tech.)

Electrical Engineering, is it a boon or curse?
Or maybe it is simple, say, to sing it in a verse:
Capacitors and Inductors at odds in every way,
But power in both cases does not dissipate away;
Hail the good ol' resistor - your equations are so simple,
Yet, when you get nasty, 'pop' bursts the students' bubble;
Then come diodes, and exponentials and logarithms enter!
What's a single diode? There are two in a transistor.
So, I say to the students, at the cost of sounding cliché
Watch out guys, En Garde, Touche.

Internship Diaries

Here is what Neel Shah (4th year DD – CSP) did while he was an intern at IST, Austria

I was an intern at the Institute of Science and Technology, Austria this summer. The institute is still in its infant stages, since it started in 2008, with only 16 research groups when I was there. It is situated in a small town called Klosterneuberg to the north of Vienna, and is surrounded by woody hills, with the river Danube nearby. The hills are a great place to walk around on a lazy evening. The whole environment creates an ideal setting for academic stimulation. The institute itself is modelled on philosophies to encourage more interdisciplinary research, not only among trivially overlapping fields. We used to have a weekly seminar which everyone in the institute would attend, irrespective of their field of study. This was followed by free food and alcohol, the aim being to get people, usually from radically different backgrounds, say topology and neuroscience, to start having informal discussions which could possibly lead to exciting collaborations. There were no undergraduates (except other interns), so almost everyone was at least a couple of years older than me, but that didn't really make a difference. Needless to say, most of the people I met were interesting people, partly due to the eccentricity that tags along with being an academic.

Regarding my own work, I was with the Computer Vision and Machine Learning group. I worked on creating an Object Detection System based on previous state of the art work, and then using it for experimenting on refined algorithms which relied less on heuristics. For my project, I essentially had to read a lot of papers and code. Apart from that, I was part of two reading groups, where we, well, read books and papers and presented to the group. This turned out to be a lot of fun as I got to explore a relatively new field with tons of cool math. On a developmental level, I improved my skills in coding, scientific presentation and exchanging abstract ideas, among other things.

Spending three months in a foreign culture goes a lot into broadening your world – views. I got the chance to roam around a bit of Germany, Austria, Italy and Amsterdam during the weekends. Moreover, Vienna is no less than paradise if you are even mildly interested in any of the arts. It has a throbbing music scene, with lots of live music venues. I spent most of my Friday nights going to a variety of gigs spanning blues, jazz, alt rock, classical, post rock and even an opera. The museums in Vienna have exhibitions ranging from the Renaissance to more modernist and post-modernist movements. Moreover, the people are in general, extremely friendly, in that anyone you make eye-contact on the street with will smile back at you, something which we are not used to experiencing in this country.

All in all, it was a really good experience. I figured out that science was actually as cool as I perceived it to be for a career, met people with different perspectives in life, learned the pleasures of wine, backpacked across European cities and made friends halfway across the globe. Wouldn't say there was anything to complain about.

Sabareesh Nikhil (2nd year – B.Tech.) talks about his internship experiences after 1st year

The power of the future – nuclear fuel doesn't avail itself to us all that freely. And when two giants in the scientific realm of the nation come together to define the future, it is hard not to be honoured to be a part of it all.

Infinite lukkhapan and doctor's advice to stay away from games for a while drove me to apply to an industrial training programme at the Electronics Corporation of India Limited (ECIL), Hyderabad. The programme was to last a month, and despite not being awarded with any fixed stipend or reimbursement for miscellaneous expenses, I was given great insight into the working of the mechanism behind nuclear fuel purification as is undertaken at the Bhabha Atomic Research Centre (BARC).

Assigned a project in the Pulsed Power Supply division, I was introduced to some state-of-the-art facilities, and exposed to ingenious methods of exploiting them. The work of the division encompassed developing and improving upon existing machinery to purify the nation's uranium and convert it into fissile material, which is later employed by BARC.

Conversion of impure uranium to its hexafluoride, which may later be processed easily to obtain enriched uranium, requires sudden bursts of focussed high power pulses. Copper vapour lasers responsible for production of such pulses are completely automated. The circuitry comprised an SMPS (switched-mode power supply) followed by extensive filtering and pulse concentrating successively. I also learnt to work on a Programmable Logic Controller (PLC), and developed part of the code used to control air flow using ladder logic.

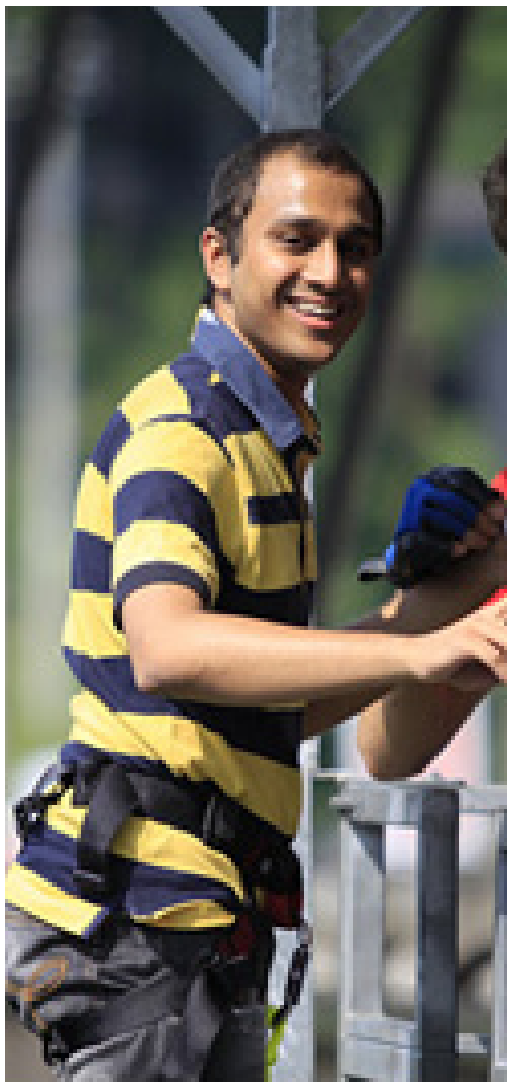
Further, I was taken around various departments, and introduced to the working of many of them in a concise and crisp manner by my trainer. The way simple concepts were intelligently applied in most of them appealed to me.

An interesting month that was; the certificate I was handed at the end hardly suffices to be a souvenir to that very educative and enjoyable experience!

Vashist Avadhanula (4th year – DD-CSP) talks about his internship experience at Sony, Tokyo

My experience at Sony, Japan was a first of its kind in many aspects; it was my first exposure to earthquakes (8 in 11 weeks!), an industrial experience and a foreign land. The internship at Sony was a quite an enjoyable one for me, both from work and sightseeing perspectives; I worked on some particular class of Image processing algorithms, with a very little experience in image processing before going there. My work basically involved experimenting and improvising an original algorithm designed by a Stanford professor, so as to help Sony implement it in a Digital Camera. It involved a fair amount of coding in C++, but the key part of the internship was to understand 3-4 research papers related to my work, implement a particular algorithm and fine tune it to get better results. The other interns (1 from IITB and 4 from IITD) work was pretty much coding based; while a couple of them got to work on CMOS image sensors (I'm not sure of the exact terminology).

I was selected after an interview for which I was shortlisted based on a couple of essays related to my internship and resume. My interview was more of an HR kind and the HR was particularly impressed with my SOP's and my academic record.



The stipend paid to me was sufficient for my 11 weeks stay; I saved a good amount even after travelling every week end and eating outside very often! Japan is a beautiful country and offers a lot to tourists! I faced a little problem finding vegetarian food, particularly on weekends (During week days, lots of Indian restaurants are open near my office building), this is not a serious problem if your work place is in Tokyo, but this can be a very serious problem if your place of work is not Tokyo. The other problem I faced during my internship was that Sony was very particular about being punctual, we were not allowed to take a single holiday unless and until you are ill, you might wonder if it is a big deal, but trust me it does take away a little freedom from us.

If you ask me if one should consider interning at Sony seriously, well I don't have a definite answer, only because of the fact that Sony opens its internship profile very late (late January), which according to me is a bit risky to stay without an internship till then. Even you consider it seriously, there is no guarantee that you get selected for the internship, as the selection depends on various factors and not just on CPI, but if you end up getting an internship at Sony, consider yourself lucky, because this is the best core internship one can get in and you will have very good chances of getting a PPO too! ■

An Educated Potter

Uttam M. Pal (2nd year M.Tech. – Control and Computing)

Two years ago, I had visited a seminar on 'Electronics and Communication Instruments'. As we were waiting for the speakers to arrive, suddenly we were interrupted by a young candidate. He began, "I am here to give you a presentation on opportunities that you have after graduation so if you are ready then we can begin". The audience including me agreed reluctantly. So he continued, "Thank you for giving me this opportunity, I wish to tell you a story: I went to my village Jitpur and there I met a kid around 10 years old. I thought he was a potter and asked him why he didn't get educated. The school was providing education at a nominal fee. His elder brother came from behind. Please dada, what is the need of education, after 10 years also he is going to make pots, what is the need of education", "Podha Shuna thike kichu hobe na" I was stunned by the truthful reply and didn't have anything solid to say to counter that reply. I saw the cold shining eyes of the kid. I shamefully returned without an answer for my own question.

"I returned home to Gujarat and that reply still haunted me and so I met my Guru, Michael Godard Wilson, a mathematician and presented the problem to him. He explained: "Son, there are two kinds of potters: an uneducated potter and an educated potter. The uneducated potter will only know how to make pots, only pots nothing else. The chief material used to make pots is mud. The educated potter will think creatively and may use the same mud to make maybe a cup, a seat, a sculpture or even a house! And an intelligent potter would remove the silicate and make a piece of glass. You know that is the difference". After returning to my home, I reflected: "An uneducated potter is analogous to an uneducated graduate. We study electronics in our college for 4 years which is nothing but what that potter kid did. We know just to make pots i.e. electronic devices.

The Educated Graduate can apply his knowledge of electronics to a myriad fields such as medicine, automobile, music, irrigation and farming, et al. It is our decision what we wish to become – an educated graduate or an uneducated potter". "Thank you for giving me this opportunity and bearing me for so long. Good Luck!" We all went clapping loudly, but only few absorbed the real meaning of the story. I did. ■

Word From Us

As its name suggests, the primary aim of this magazine is to bring the hum in the background to the fore, i.e. to present the fascinating research being done by the students and Professors of Electrical Engineering Department, IIT Bombay. We hope to generate interest, especially among undergraduate students, about new and upcoming areas of technology, and encourage more and more post graduate students to explain their research work. With these objectives in mind, we have tried to include articles from a broad spectrum of fields, ranging from Power Electronics, VLSI Technology to Communication Systems and Image Processing. With careful scrutiny, we have strived towards maintaining authenticity and honesty in all the articles and images that we have published. We also aim to provide the readers an update of various activities organised by EESA this semester. We have also introduced a couple of new sections – 'Leisure', containing light reads and 'Internship diaries', through which a variety of internship experiences have been shared. The authors have tried to explain the technicalities of their field as simply and succinctly as possible. We would like to thank everyone wholeheartedly who has helped us in bringing this issue out. Any feedback/suggestions from you are most welcome! ■

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